ELECTROSTATIC CHUCKS

Rf Chuck Edge Design

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This document addresses the following chuck edge design issues:

- Device yield through system uniformity and particle reduction;
- System maintenance through edge cleanability and wafer retention;
- Plasma - chuck electrical interactions due to chuck electrode design.

indicates where we describe Electrogrip product features.

These documents are "works in progress" and will be updated from your comments and questions.

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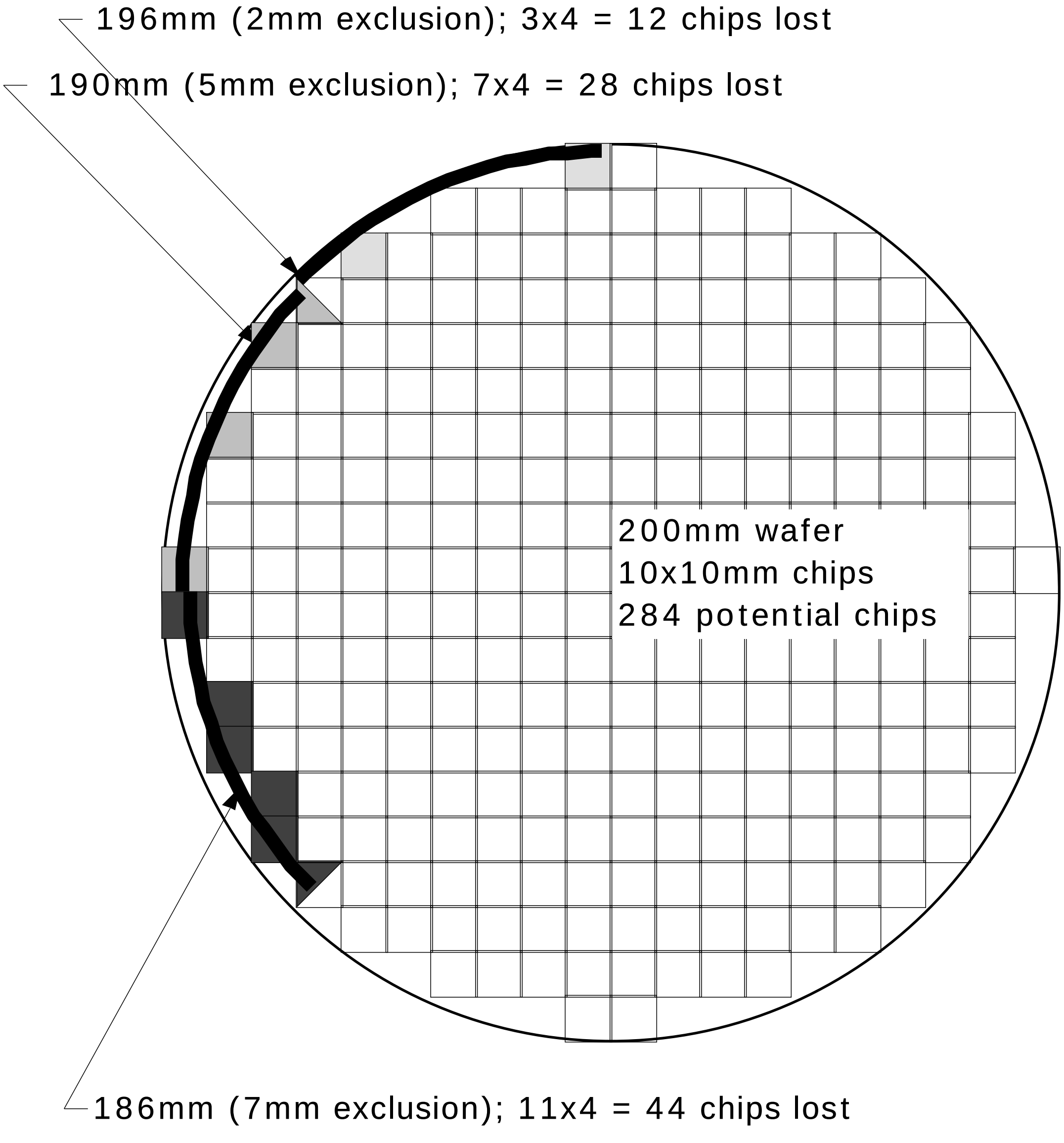
1. EDGE YIELD

- See below for the geometry assumed here. 100mm^2 chips on a 200mm dia. substrate are representative of memory and microprocessor devices.
- For 1 wafer processed every 2 minutes, and for chips worth $20, the edge exclusion hourly losses are:

$7,200	for a	2mm exclusion zone;
$16,800	for a	5mm exclusion zone; and
$26,400	for a	7mm exclusion zone.

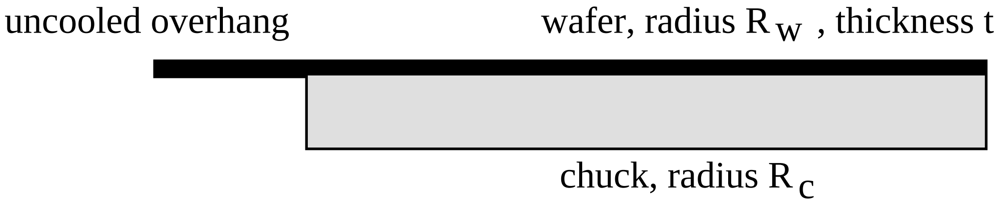
- Attaining edge yield requires that all processing machines allow processing to the edge, from resist spinning edge bead to plasma machines to furnace supports.

EDGE LOSSES OF CHIPS



2. OVERHANG THERMAL EFFECTS

- Assume a wafer exposed to a uniform plasma heat source of power P to wafer.
- Vertical heat conduction through wafer to chuck over chuck surface, except at edge.
- At the edge cooling is poorer and lateral heat flow through the wafer occurs, with consequent higher edge temperatures.
- High edge temperatures result in altered deposition conditions and wafer hoop stress.
- An idealised calculation is shown below.



Assume no radiative loss (all heat is sunk to chuck).
For T_w = wafer edge temperature and T_c = wafer temp. over chuck:

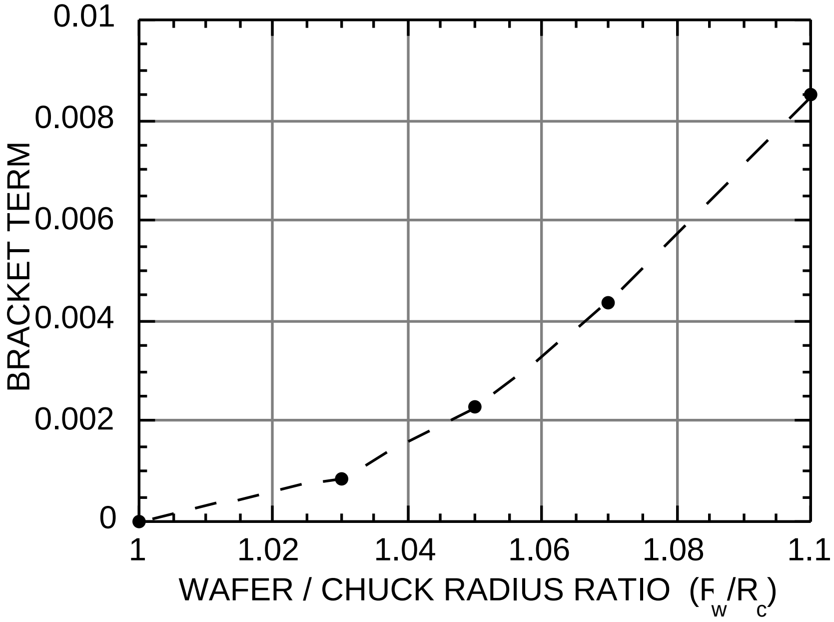
$$T_w - T_c = \frac{P}{4\pi\kappa t}\left\{ \ln(R_w / R_c) - 0.5 + R_c^2 / (2 R_w^2) \right\}$$

where P = total power to wafer and κ is the wafer thermal conductivity.
The curly-bracketed term is shown graphically below.
The first term, for Si with κ = 100 W/(m-K) and t = 0.5mm, is ~3 P (W).
For 150mm wafers with 140mm chuck dia. the radius ratio is 1.07;
for 200mm wafers with 190mm chuck dia. the radius ratio is 1.05.

Typical values for 5mm overhang:

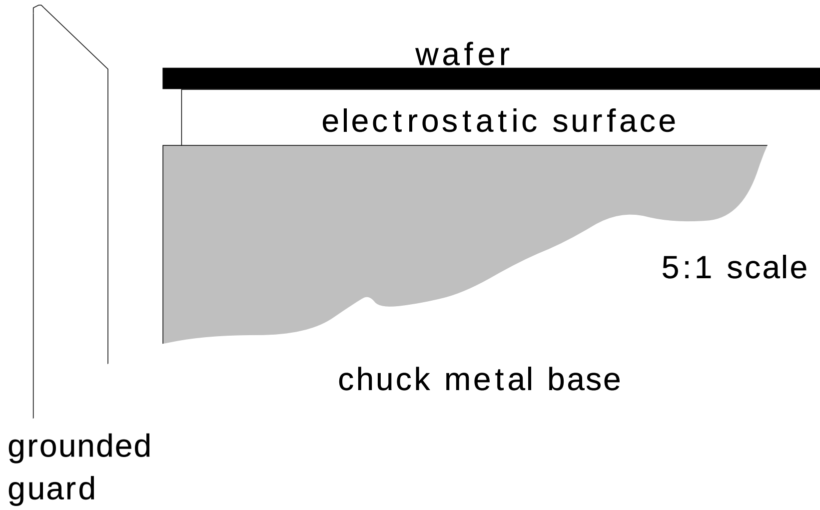
P=100W, ΔT=1°C

P=1kW, ΔT=10°C.



3. SIMPLE OVERHANG CHUCK

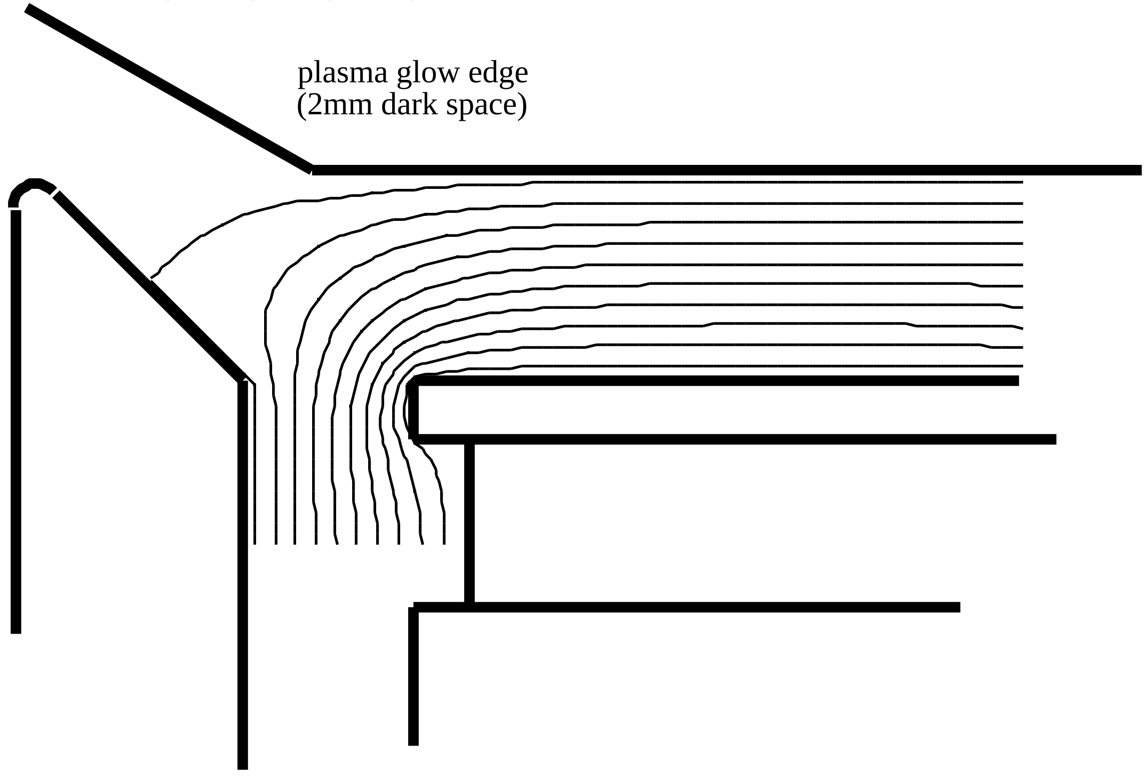
Diagram



Field plot

(-200V bias on wafer, +20V plasma potential with respect to grounded guard)

- ions, mainly from the glow edge at low pressures, are accelerated normal to the field lines. Thus ions start at glow edge and generally bombard normal to the wafer surface.



Wafer retention

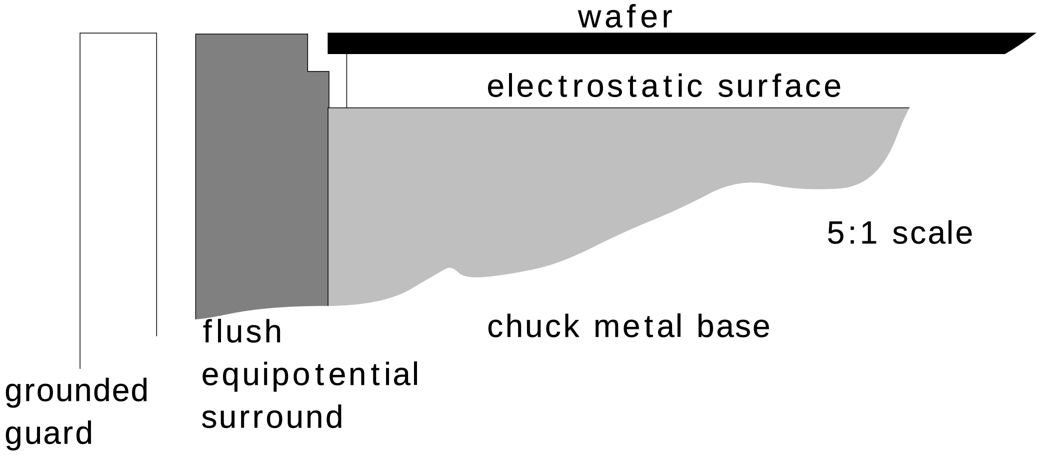
- Guard ring retains wafer in case of slippage from chuck surface.

Plasma effects

- Edge of wafer is more heavily ion-bombarded than center due to ion lensing. Plasma extends around edge; may etch / coat on wafer edge and underside, and chuck side.
- Cleaning: chuck minimally; guard regularly to minimise particles in deposition processes.

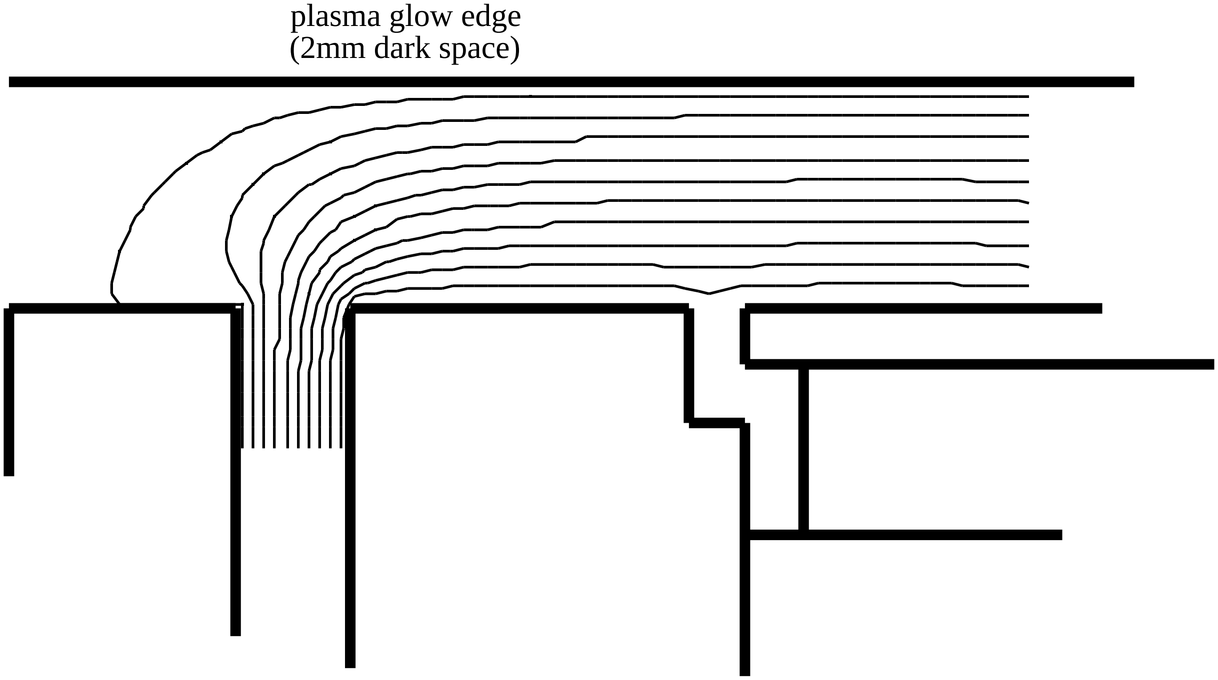
4. FLUSH CONSUMABLE RING

Diagram



Field plot (-200V bias on wafer, +20V plasma potential with respect to grounded guard)

- ions, mainly from the glow edge at low pressures, are accelerated normal to the field lines. The dark space in these diagrams is the ion acceleration space between plasma and wafer.



Wafer retention

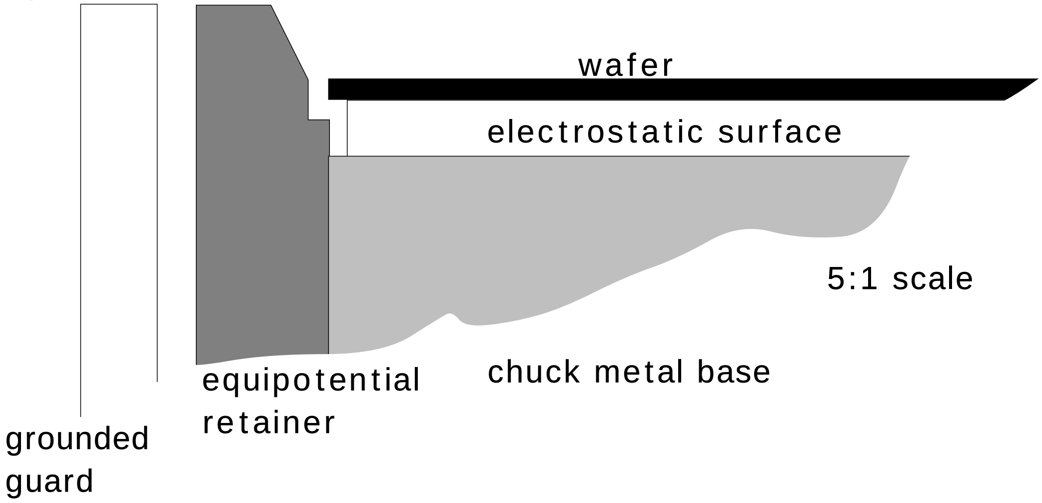
- Recess in surround ring retains wafer by thickness of wafer only. Guard ring, if raised in height, could retain wafer in case of slippage from chuck surface.

Plasma effects

- Very uniform wafer ion bombardment if surround ring rf impedance is matched to chuck.
- Cleaning: Chuck minimally; Guard and surround ring regularly to minimise particle generation in deposition processes.
- Replace surround ring when etched below wafer thickness mid-point. Surround ring etch products contribute to etch process chemistries.

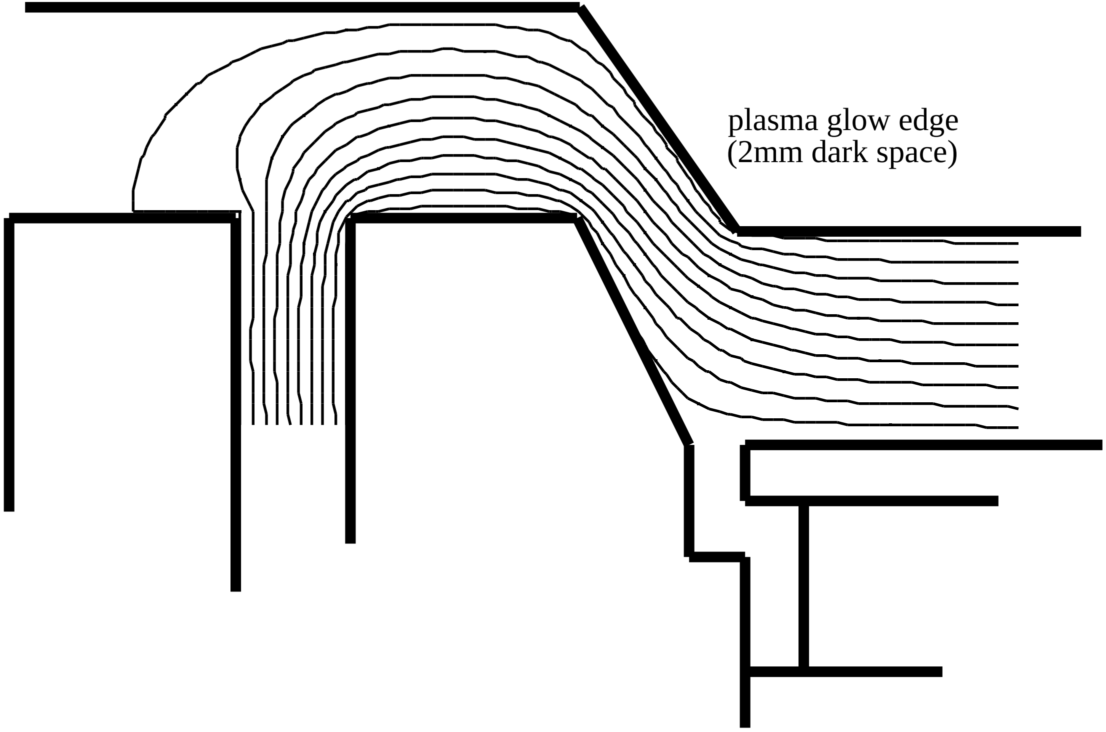
5. RETAINER RING

Diagram



Field plot (-200V bias on wafer, +20V plasma potential with respect to grounded guard)

- ions, mainly from the glow edge at low pressures, are accelerated normal to the field lines.



Wafer retention

- Retainer ring retains wafer in case of slippage from chuck surface.

Plasma effects

- Lighter wafer ion bombardment at edge compared to center due to ion lensing. Plasma may etch or coat on retaining ring. Plasma particle trap inside ring possible.
- Chuck surface is not consumable. Chuck requires little if any cleaning. Clean the retaining ring to minimise particle generation in deposition processes.
- Replace retaining ring when severely etched. Retaining ring etch products contribute to etch process chemistries.

6. PLASMA-CHUCK ELECTRICAL INTERACTIONS

- *Plasma contact induces bias* A surface in contact with plasma and capacitively coupled to outside circuitry (such as an rf sputtering target) will equilibrate to a negative voltage with respect to the plasma. Plasma electrons have higher energy and velocity than plasma ions. Thus electrons can overcome the negative voltage and arrive with a current equal to that of the ions.
- *Rf voltage induces more bias* If rf voltage is applied to the surface then the average negative voltage with respect to the plasma (typically comparable with the "rf bias voltage") is raised to about half of the rf peak-to-peak voltage. In positive half cycles, electrons are pulled quickly to the surface and fully discharge the surface. When the rf voltage goes negative, electrons are repelled. Ions arrive (more slowly) to neutralise the electron charge.
- *Rf plasmas use high currents* Typical substrate currents in high density plasmas are of the order of amperes for 200mm dia. susbtrates. Low density, low pressure "RIE" plasmas still reach 100mA current levels. These currents can easily be verified by shorting a conducting target's induced dc bias to ground through a current meter. The induced plasma bias on targets is typically between 100V and 1kV, yielding a "resistance" to dc current flow on 200mm substrates of the order of 500V / 1A = 500Ω.
- *Plasma edge conduction* At target edges there is reduced plasma penetration through small gaps (typically 1mm wide and 2mm deep) to underlying target metal electrodes. If metal contact area is further reduced for low plasma contamination, plasma bias source impedance can reach many megohms, requiring a high impedance bias sense circuit.

Electrogrip DR4 drivers typically have a 68MΩ bias sense impedance. This impedance can be increased if desired.

- *Electrostatics use low currents* Typical electrostatic gripping power supplies deliver 700V through 1MΩ resistance to anodised Al grip electrodes, and 4kV through 20MΩ resistance to thicker dielectrics such as those used by Electrogrip. Hence available current levels are lower than 1mA.
- *Electrode contact with plasma* If the conductive plasma contacts one of the gripping electrodes then grip forces and the plasma will be affected. The same negative bias will be induced on both gripping electrode and substrate, with a resultant low gripping force.
- *Avoidance of electrode contact* Isolation of gripping electrodes from plasma is generally preferred. Such designs may be monopolar, bipolar, tripolar, etc. , and use gripping electrodes which are embedded in insulator on all sides or protected from plasma with a metal shield electrode.
- *Electrode contact can be good* In tripolar chuck designs using floating gripper power supplies, <u>the third tripolar electrode must contact plasma</u> to provide a bias voltage reference for the gripping power supply.

Electrogrip rf chucks are tripolar, with two gripping electrodes embedded inside insulator and totally inaccessible to the plasma. The third electrode is a metal shield, additionally blocking plasma from the gripping electrodes.

Plasma contact to the baseplate electrode yields an rf bias voltage which is filtered in the BD2 bias decoupler and then fed on the high voltage cable shields to the DR4 driver.

The gripping electrode voltages are also filtered in the BD2 bias decoupler since they are capacitively coupled to the baseplate rf potential. This ensures that gripping potentials are referenced to the true instantaneous rf substrate potential, for a constant gripping force independent of rf plasma voltage.

7. SUMMARY

Edge Uniformity, Process Cleanliness

There is no universal "best" solution to the edge uniformity / process cleanliness tradeoff. Chuck edge design is determined by chuck accessibility for routine maintenance and on the proposed process.

Examples:

- an inaccessible chamber used for deposition would favor the edge overhang design;
- an accessible chamber used for etch processes would favor the flush surround ring design;
- where wafers are likely to slip off the chuck surface due to vibration or process irregularities, the edge overhang or retaining ring designs are preferred;
- if wafer lift timing is not well synchronised with grip and release timing, in the edge overhang design wafers may slip and short against the guard ring.

Electrogrip chucks can be made in all of the varieties shown.

CHUCK EDGE DESIGN CHOICES

TYPE:	**Edge Overhang**	**Flush Surround**	**Retaining Ring**
PROPERTY			
Ion bombardment uniformity	Poor (high at edge)	Excellent	Poor (low at edge)
Temperature uniformity	Poor (high at edge)	Good (high at edge)	Excellent
Chuck edge bombardment	Low	Low-zero	Low-zero
Edge material bombardment	Low	High	High
Deposition: Clean frequency	Low	Med	High
Cleaned parts	Guard	Guard, Ring	Guard, Ring
Lateral wafer retention	Good	Poor	Good
Synchronised wafer lift	Required	Not required	Not required

Plasma Contact to Gripping Electrodes

Plasma contact to the gripping electrodes must be avoided. However in tripolar designs plasma contact to the third baseplate electrode is required for correct operation.

Electrogrip provides integrated systems of chucks, bias decoupler filters, and floating high voltage drivers. These systems yield a grip force independent of plasma parameters. Electrogrip systems have no plasma degradation of grip force, and no grip electrode interference with the plasma.